MAY 10 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Hawks, et al.
Serial No.: 10/649,577
Filed: August 26, 2003
Art Unit: 2822
Examiner: Trinh, Michael M.
Title: Methods Suitable for Forming a Microelectronic Device Package

DECLARATION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

I, Robert J. Terry, declare as follows:

1. I am the Assistant General Counsel/Assistant Secretary at Skyworks Solutions, Inc., which is the owner of the above-referenced patent application.

2. I declare that, as detailed in the enclosed Innovation Disclosure, the inventors of the above-referenced patent application conceived the invention of the above-referenced application, as defined by its pending claims, in the United States, on or prior to September 22, 1998.

3. To evidence conception of the invention of the above-referenced application in the United States, attached hereto, please find a copy of the Innovation Disclosure submitted by the inventors of the above-referenced application, which describes the invention of the above-described patent application in Docket No. 98RSS411, entitled "Process for Fabricating an Area Array Semiconductor Package", which was entered into the Innovation Disclosure Database, on September 22, 1998.

4. I declare that, as evidenced in the Innovation Disclosure and also by filing of the parent of the above-referenced patent application in the USPTO, on October 11, 1999, the invention of the above-referenced application was reduced to practice in the United States using due diligence after conception.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine of imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced patent application or any patent issuing thereon.

5-10-2006
Date

Robert J. Terry
Assistant General Counsel/Assistant Secretary
Skyworks Solutions, Inc.

Innovation Disclosure

Docket No.: 98RSS411
Ranking: APPROVED TO FILE

1. Innovator(s)

Name	SSN	Dept.	Mail Code	Telephone	Supervisor
Doug A Hawks		529	San Diego 581	(619)597-4402	Hassan S Hashemi

2. Title of Invention

Process for Fabricating an Area Array Semiconductor Package

3. Problem Solved

Typical area array packages, like plastic ball grid arrays, are substantially more expensive than equivalent pincount leadframe based packages. Often the BGA substrate cost is the dominant factor in total package and assembly cost. This disclosure provides a process by which a BGA or LGA package may be fabricated using standard leadframe packaging materials, thus substantially improving the final package cost. The final package configuration offers improved thermal and electrical performance over standard PBGA and other chip scale packages.

4. Previous Solutions

Some suppliers have used polyimide tape as the carrier substrate for the package, requiring vias and expensive tape. Others, such as Fujitsu use a different process for fabricating their Bump Chip Carrier, ending with a structure similar to that proposed in this invention.

5. Solution

Please refer to attached figure.

A process is described for fabricating an area array semiconductor package.

Step 1 - Standard lead frame material (copper) is laminated to a polyimide (or other organic carrier tape). The leadframe is silver plated in the areas that will be wirebonded later in the process. The leadframe is coated with photo resist for normal patterning operations. The tape may be used as the carrier throughout the assembly operation, as is common with tape automated bonding packaging. Packages are processed multi-up in strip format as typical of any leadframe package assembly process.

Step 2 - The photo resist is patterned for the final interconnect structure.

Step 3 - The unwanted copper is etched, leaving only the pattern defined by the photo resist mask. Note - Undercutting of the copper metallization is acceptable, even desireable, allowing the metal traces to be mechanically locked into the mold compound during the molding process, as defined in step 6.

Step 4 - The photo resist is stripped, exposing the silver plated copper pattern.

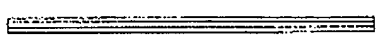
Step 5 - Die attach and wirebond are now performed.

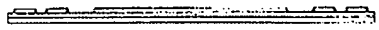
Step 6 - The package strips are now molded using standard mold processes. Marking and mold cure are performed.

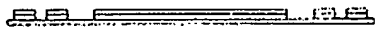
Step 7 - The polyimide tape is removed from the package.

Step 8 - The package strips are now sawn into individual packages.

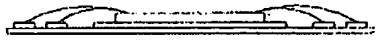
Step 9 - Shows a top view of the completed package. The completed package has the following features.
1) Fine pitch BGA or LGA configurations
2) Small body size
3) Cost similar to leadframe based packages (ie. TQFP)
4) Low thermal impedance due to direct attachment of die to copper pad, which can be soldered directly to customer application board.
5) Enhanced electrical performance - no internal package signal routing. Wirebonds connect directly to copper IO pads. Low impedance ground
path available if downbond is performed to die attach pad.
6) Low profile (<= 1.0mm height)
7) Low weight
8) Improved solder joint reliability due to minimized stresses between mold compound and leadframe and PCB.
9) Compatible with existing standard package assembly operations. The only non-standard process is polyimide tape removal.

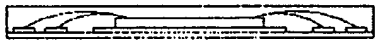

Step 1 - Leadframe laminated to polyimde tape, coated with photo resist.

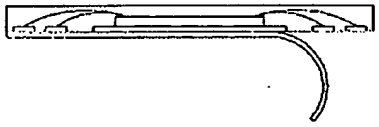

Step 2 - Pattern photo resist

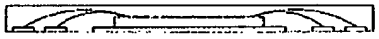

Step 3 - Etch copper pattern

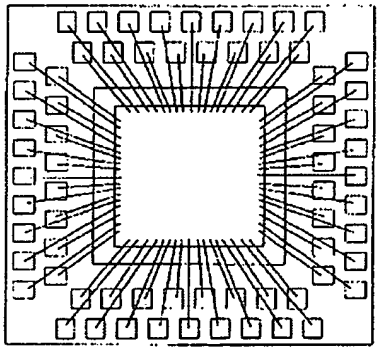

Step 4 - Strip photo resist


Step 5 - Die attach and wirebond


Step 6 - Mold, cure and marking


Step 7 - Remove polyimide tape


Step 8 - Singulation using saw process


Step 9 - Completed package: top view

6. Differences/Advantages Over Previous Solutions

This invention utilizes standard materials and processes. The leadframe supplier should provide the leadframe with pattern design, ready for package assembly. Other solutions utlize costly substrate materials, such as patterned polyimide with vias, or BT resin, or require expensive processing in the assembly factory. This package process will fit into most standard assembly operations.

7. Status of Innovation

Idea If "Other", please specify

8. Product or program in which Innovation will be used:

This package would be suitable for most Rockwell products requiring small package size, enhanced thermal and electrical performance,
and low cost.

9. Has anyone disclosed or does anyone plan to disclose your innovation outside the Company?

○ Yes ● No ○ Don't Know
If "Yes", where:

10. Has anyone proposed or does anyone plan to propose a product or program to a customer which includes your innovation?

○ Yes ● No ○ Don't Know
If "Yes", when and how:

11. Innovator signature(s): (Do not use black ink)

_____ **Date** _____

Qtr Evaluated: 4Q98
Group: Platform Technologies
Technology:
Sub Technology 1:
Sub Technology 2:
Products:

Entered: Doug A Hawks @ 09/22/98 03:13 PM
Modified: Donna Bastedo @ 04/28/99 05:36 PM

Revision History:
Revised: 23-Sep-1998 10:10 AM by Donna Bastedo
23-Sep-1998 01:53 PM by Doug A Hawks
24-Sep-1998 09:56 AM by James K Dawson
24-Sep-1998 11:19 AM by James K Dawson
28-Apr-1999 05:36 PM by Donna Bastedo